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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,527	11/30/2001	Peter J. Melsa	TI-33111	6081

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2644	8

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/997,527	MELSA, PETER J.	
	Examiner	Art Unit	
	Walter F Briney III	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time mey be availeble under the provisions of 37 CFR 1.136(a). In no event, however, mey a reply be timely filed after SIX (6) MONTHS from the meiling dete of this communicetion.
- If the period for reply specified ebove is less then thirty (30) deys, e reply within the statutory minimum of thirty (30) deys will be considered timely.
- If NO period for reply is specified ebove, the meximum statutory period will epply end will expire SIX (6) MONTHS from the meiling dete of this communication.
- Feilure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office leter then three months efter the meiling dete of this communicetion, even if timely filed, mey reduce eny eerned petent term edjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-24 and 26* is/are rejected.

7)☒ Claim(s) *5,8 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 5 is objected to because of the following informalities:

- A period is missing at the end of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1, 5, 6, 7, and 18-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujiwara (US Patent 4,873,493).**

Claim 1 is limited to *a line driver*. Fujiwara discloses an audio amplifier (abstract; figure 11), the amplifier drives an audio *input* (21) out to an output port (28), because the audio amplifier is intended for use in a CD player, the port inherently connects to an audio transducer by way of a wire or line (i.e. the audio amplifier is a *line driver*). As can be seen from figure 11, one of the digital input signals (21) is selected to be amplified by selector (22), it is interfaced to the amplifier by DIR (23). The peaks of the input selected input signal are detected by control unit 40' containing a peak detector (42). Figures 3A-3D illustrate the timing of the control circuit disclosed by Fujiwara. When an

input signal (a), as seen in figure 3A, breaches an established threshold (Vc), a control pulse (c), as seen in figure 3C, is generated by the comparator circuit of figure 11 (i.e. *a peak detector receiving a digital data signal from the signal input and outputting a logic signal having a first logic value when the digital data signal exceeds a threshold value*). Otherwise, the control signal (c) is low (i.e. *and a second logic value when the digital data signal is below the threshold value*). In the design of the audio amplifier, the threshold value used by must be programmed. Inherently, the value of the threshold is determined based on some type of overhead that is determined through analysis. Furthermore, Fujiwara discloses selecting a threshold for the comparator (53) such that a maximum output with minimal distortion under the lesser of the two possible supply voltages is produced (column 6, line 65 to column 7, line 4). Fujiwara also discloses delaying the audio signal path with a delay circuit (24) (i.e. *a data signal delay*). Fujiwara also discloses converting the input signal to the analog signal domain prior to amplification (25) (i.e. *a DAC coupled to the signal input and receiving as input the time-delayed digital data signal and outputting an analog data signal*). The output of the D/A converter used by Fujiwara is variably attenuated by circuit 26 (i.e. *a filter receiving as input the analog data signal and outputting a filtered analog data signal*). Finally, the input signal is amplified by power amp 27 (i.e. *and an amplifier receiving as input the filtered analog data signal from the filter*). As can be seen, the power provided to the amplifier is a function of the peak detecting circuit (42). When the input signal is above the threshold a high operating voltage is supplied, but when the input signal is below the

threshold a low operating voltage is supplied (figure 6; column 6, line 65 to column 7, line 9). Therefore, Fujiwara anticipates all limitations of the claim.

Claim 5 is limited to *the line driver of claim 1*, as covered by Fujiwara. The peak detector (figure 11, element 42) used by Fujiwara is part of a complex analog signal *processor* (40'). Any process performed by this processor is a *routing*. Therefore, Fujiwara anticipates all limitations of the claim.

Claim 6 is limited to *the line driver of claim 5*, as covered by Fujiwara. Fujiwara clearly depicts in figure 3D that the logic signal used to control the available power levels is held for a time denoted as "td," which represents the amount of time necessary to maintain the high voltage level. Therefore, Fujiwara anticipates all limitations of the claim.

Claim 7 is limited to *the line driver of claim 1*, as covered by Fujiwara. Fujiwara discloses generating a signal V_1, which is the output of the peak detector. Furthermore, a peak prediction signal known as V_o is also created as a function of V_1, and hence, a function of the input (column 6, lines 36-40) (i.e. *further including a peak predictor for receiving the digital data signal from the signal input and outputting an intermediate control signal*). Therefore, Fujiwara anticipates all limitations of the claim.

Claim 18 is limited to *a line driver system*. The system of claim 18 is anticipated by the limitations set forth in claim 1, as covered by Fujiwara, with the exception of *a transmission line coupled to an output of the amplifier; and a receiver coupled to an output of the transmission line*. While Fujiwara does not illustrate the presence of a transmission line and a receiver, the fact that the amplifier is used for amplifying audio

for, for example, CD players an inherent connection between the amplifier and an output transducer exists. Therefore, Fujiwara anticipates all limitations of the claim.

Claim 19 is limited to *the line driver system of claim 18, wherein the overhead is a programmable value*.

Claims 20 and 21 are essentially the same as claims 3 and 4, respectively, and are rejected for the same reasons.

Claims 22 and 23 are essentially the same as claim 6, and are rejected for the same reasons.

Claim 24 is limited to *the line driver system of claim 18*, as covered by Fujiwara. This claims includes the circuitry described in claim 7 plus the function described in claim 16, both of which are disclosed by Fujiwara. Therefore, Fujiwara anticipates all limitations of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara.

Claim 9 is limited to *the line driver of claim 1*, as covered by Fujiwara. As explained in claim 1, Fujiwara discloses setting the threshold in order to minimize distortion while using the lesser of the available supply sources, clearly, determining the minimum distortion is done either by making analytical predictions or by observing effects of various trials. In either case, Fujiwara does not disclose how to determine the o*verhead value*, and thus anticipates all limitations of the claim with the exception *wherein the overhead value is determined empirically*. The examiner takes Official Notice of the fact that determining parameters of a design by empirical methods is well known. It would have been obvious to one of ordinary skill in the art at the time of the invention to determine the overhead value for the threshold based on empirical methods because empirical evidence provides a feedback that can account for real-life variables that are too complicated to consider in more analytical approaches.

Claim 26 is essentially the same as claim 9 and is rejected for the same reasons.

3. Claims 2-4 and 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara in view of Myers et al. (US Patent 5,929,702).

Claim 2 is limited to *the line driver of claim 1*, as covered by Fujiwara. Fujiwara discloses using two different voltage supplies depending on the level of the input signal, which could lead to an inefficient use of power when the input signal varies between multiple levels of sustained volume. Therefore, Fujiwara anticipates all limitations of the claim with the exception *wherein the peak detector outputs a third logic value when the digital data signal exceeds a second threshold value and further wherein the amplifier*

operates at a third operating voltage level when the peak detector outputs said third logic value. Myers teaches an envelope detector coupled with a comparison device that controls the generation of two different voltage supplies for use by a power amplifier (abstract; figures 1, 2, 3). This configuration is similar to that used by Fujiwara, however, Myers also teaches that more than two levels can be used (column 5, lines 6-16), the effect is an inherent increase in power efficiency because the closer the available power ceiling is to the level of the input signal the less wasted power there is. It would have been obvious to one of ordinary skill in the art at the time of the invention to include more than two power levels as taught by Myers for the purpose of reducing wasted power in a power amplifier by using narrow power supply ceiling to input signal level margins.

Claim 3 is limited to *the line driver of claim 1*, as covered by Fujiwara. Fujiwara includes a digital delay circuit (figure 11, element 24) to insure that the power available to the amplifier (27) has had enough time to be adjusted before the presence of the input signal has reached the input of the amplifier. However, upon analysis of figure 3A-3D, it is apparent that the power level available to the amplifier is ready well before the arrival of the input signal at the amplifier's input. The symbol "tc" represents the switching time to alternate between a low and high voltage. The symbol "td" represents the time until the input peak arrives. Clearly, they are unequal. Therefore, Fujiwara anticipates all limitations of the claim with the exception of *a logic delay receiving as input said logic signal and outputting a time delayed logical signal*. Myers, teaches equalizing the delay between an envelope and phase portion of an input signal that is to

be amplified by a power amplifier (figure 1, element 260; column 2, lines 60-67). Clearly, equalizing the delays reduces any time where excess power is being supplied, such as the difference between "td" and "tc" disclosed by Fujiwara. Because the switching time of the amplifier is fixed, the only way to resolve the delay issue in Fujiwara would be to delay the logic signal used to trigger the power supply switching. It would have been obvious to one of ordinary skill in the art at the time of the invention to delay the switching command of Fujiwara in order to equalize the path delays as taught by Myers, and thus, a reduction in wasted power is achieved.

Claim 4 is limited to *the line driver of claim 3*, as covered by Fujiwara in view of Myers. In order to equalize the path delays, all variables imposing phase inequalities must be considered, so that the delay imposed on the digital signal must inherently equal the difference between *the delay imposed by the filter and the switching speed of the amplifier*. Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim.

Claim 10 is limited to *a method of operation of a line driver*. The method steps of claim 10 are inherently performed by the line driver of claim 1 with the exception of using a *programmable digital data signal delay value*. However, like shown in claim 3, an alternative to the fixed time delay used by Fujiwara, both paths can be controlled so that the difference in their processing times can be equalized, which results in a reduction of wasted power. It would have been obvious to one of ordinary skill in the art at the time of the invention to equalize the delays of both the amplification path and the

peak detecting path using variable (i.e. programmable) delay paths as taught by Myers, which result in a reduction of wasted power.

Claim 11 is limited to *the method of claim 10*. The amplifier disclosed by Fujiwara uses a threshold value in its comparator circuit (figure 11, element 53). The threshold value must inherently be programmed to allow operation (i.e. *further comprising programming a value for the threshold value*). Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim.

Claim 12 is limited to *the method of claim 8*, as covered by Fujiwara in view of Myers. The method steps of this claim are inherently performed by the circuitry described in the rejection of claim 6. Therefore, Fujiwara in view of Myers makes obvious all limitations of this claim.

Claim 13 is limited to *the method of claim 8*, as covered by Fujiwara in view of Myers. The method steps of this claim are inherently performed by the circuitry described in the rejection of claim 3. Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim.

Claim 14 is limited to *the method of claim 13*, as covered by Fujiwara in view of Myers. The method steps of this claim are inherently performed by the circuitry described in the rejections of claim 4. Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim.

Claim 15 is limited to *the method of claim 11*, as covered by Fujiwara in view of Myers. As presented in the rejection of claim 9, an engineer implementing the audio amplifier disclosed by Fujiwara for a particular application would use empirical methods

to determine the appropriate threshold value to be used. Temperature is an inherent modifier that affects the amount of distortion introduced by an amplifier, and would inherently be considered by the criteria set out by Fujiwara for choosing a threshold value (column 6, line 65 to column 7, line 4) (i.e. *wherein the threshold value is modified as a function of temperature*). Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim.

Claim 16 is limited to *the method of claim 10*, as covered by Fujiwara in view of Myers. Fujiwara discloses generating a peak prediction signal V_0 (column 6, lines 36-40; figure 11) using the result of a dividing circuit (51). The dividing circuit receives as input a signal V_3, which is a model of the output of filter 26 (i.e. *further comprising predicting a data signal peak based upon a model of the filtering step*). Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim.

Claim 17 is limited to *the method of claim 10*, as covered by Fujiwara in view of Myers. As presented in the rejection of claim 9, an engineer implementing the audio amplifier disclosed by Fujiwara for a particular application would use empirical methods to determine the appropriate threshold value to be used. Switching speed is an inherent modifier that affects the amount of distortion introduced by an amplifier, and would inherently be considered by the criteria set out by Fujiwara for choosing a threshold value (column 6, line 65 to column 7, line 4) (i.e. *wherein the threshold value is modified as a function of switching speed of the amplifier*). Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim.

Allowable Subject Matter

Claims 8 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 8 is limited to *the line driver of claim 1*, as covered by Fujiwara. Fujiwara discloses determining the threshold value based on distortion parameters (column 6, line 65-column 7, line 4), however, no explicit detail exists as to what type of physical effects to monitor. In claim 9, rationale supporting an empirical analysis to monitor distortion in designing the amplifier, however, this does not suggest selecting a threshold based on a comparison between a peak and an RMS value of either power supply. Therefore, Fujiwara in view of Myers makes obvious all limitations of the claim with the exception *wherein the threshold value is associated with proportionality between a peak value associated with the first operating voltage level and a RMS value associated with the first operating voltage level*. Thus, claim 8 is allowable over Fujiwara in view of Myers.

Claim 25 is essentially the same as claim 8, and is allowable over Fujiwara in view of Myers for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
8/20/04

XU MEI
PRIMARY EXAMINER